

WHAT IS CLAIMED IS:

1           1.     A differential amplifier circuit comprising:

2                   (a)     first and second supply voltage rails, first and second input terminals, and  
3     an output terminal;

4                   (b)     differentially connected first and second input transistors of a first channel  
5     type;

6                   (c)     a folded cascode circuit coupled to the first supply voltage rail and  
7     including a first cascode transistor and a second cascode transistor both of a second channel type,  
8     sources of the first and second cascode transistors being coupled to drains of the first and second  
9     input transistors, respectively;

10                  (d)     a first load transistor of the second channel type coupled between the  
11     source of the second cascode transistor and the first supply voltage rail and a second load  
12     transistor of the second channel type coupled between the source of the first cascode transistor  
13     and the first supply voltage rail;

14                  (e)     a bias source producing a bias signal on gates of the first and second  
15     cascode transistors;

16                   (f)     a third cascode transistor of the second channel type having a source  
17     coupled to a drain of the second cascode transistor and a drain coupled to a first current source, a  
18     drain of the first cascode transistor being coupled to a second current source, and a voltage level  
19     shift circuit coupled between the drain of the third cascode transistor and second load transistors;  
20     and

21                   (g)     a gain boost amplifier having a first input coupled to the drain of the first  
22     cascode transistor, a second input coupled to the drain of the second cascode transistor, and an  
23     output coupled to a gate of the third cascode transistor.

1           2.     The differential amplifier circuit of claim 1 including an output stage having an  
2     input coupled to the drain of the first cascode transistor, the output stage including a pull-up  
3     transistor of the second channel type coupled between the second supply voltage rail and the  
4     output terminal, and a second output transistor of the first channel type coupled between the first  
5     supply voltage rail and the output terminal.

1            3.     The differential amplifier of claim 2 including a class AB bias circuit coupled  
2     between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

1            4.     The differential amplifier of claim 2 wherein the gain boost amplifier is a CMOS  
2     voltage-input differential amplifier.

1            5.     The differential amplifier of claim 2 wherein the gain boost amplifier is a CMOS  
2     current-input differential amplifier.

1            6.     A differential amplifier circuit comprising:

2            (a)     first and second supply voltage rails, first and second input terminals, and

3       an output terminal;

4                   (b)     differentially connected first and second input transistors of a first channel  
5       type;

6                   (c)     a folded cascode circuit coupled to the first supply voltage rail and  
7       including a first cascode transistor and a second cascode transistor both of a second channel type,  
8       sources of the first and second cascode transistors being coupled to drains of the first and second  
9       input transistors, respectively;

10                  (d)     a first load transistor of the second channel type coupled between the  
11       source of the second cascode transistor and the first supply voltage rail and a second load  
12       transistor of the second channel type coupled between the source of the first cascode transistor  
13       and the first supply voltage rail;

14                  (e)     a bias source producing a bias signal on gates of the first and second  
15       cascode transistors, respectively; and

16                  (f)     a gain boost amplifier having a first input coupled to the drain of the  
17       second cascode transistor, a second input coupled to the drain of the first cascode transistor, and  
18       an output coupled to gates of the first and second load transistors.

1           7.     The differential amplifier circuit of claim 6 including an output stage having an  
2 input coupled to the drain of the first cascode transistor, the output stage including a pull-up  
3 transistor of the second channel type coupled between the second supply voltage rail and the  
4 output terminal, and a second output transistor of the first channel type coupled between the first  
5 supply voltage rail and the output terminal.

1           8.     The differential amplifier of claim 7 including a class AB bias circuit coupled  
2 between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

1           9.     The differential amplifier of claim 7 wherein the gain boost amplifier is a CMOS  
2 voltage-input differential amplifier.

1           10.    The differential amplifier of claim 7 wherein the gain boost amplifier is a CMOS  
2   current-input differential amplifier.

1           11.    A differential amplifier circuit comprising:

2                   (a)    first and second supply voltage rails, first and second input terminals, and  
3   an output terminal;

4                   (b)    differentially connected first and second input transistors of a first channel  
5   type;

6                   (c)    a folded cascode circuit coupled to the first supply voltage rail and  
7   including a cascode transistor of a second channel type, a source of the cascode transistor being  
8   coupled to a drain of the first input transistor;

9                   (d)    a first load transistor of the second channel type coupled between a first  
10   current source and the first supply voltage rail and a second load transistor of the second channel  
11   type coupled between the source of the cascode transistor and the first supply voltage rail;

12                  (e)    a bias source producing a bias signal on a gate of the cascode transistor;

13 and

14 (f) a gain boost amplifier having a first input coupled to a drain of the first  
15 load transistor, a second input coupled to the source of the cascode transistor, and an output  
16 coupled to gates of the first and second load transistors.

1 12. The differential amplifier circuit of claim 11 including an output stage having an  
2 input coupled to the drain of the first cascode transistor, the output stage including a pull-up  
3 transistor of the second channel type coupled between the second supply voltage rail and the  
4 output terminal, and a second output transistor of the first channel type coupled between the first  
5 supply voltage rail and the output terminal.

1 13. The differential amplifier of claim 12 including a class AB bias circuit coupled  
2 between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

1           14.     The differential amplifier of claim 12 wherein the gain boost amplifier is a CMOS  
2 voltage-input differential amplifier.

1           15.     The differential amplifier of claim 12 wherein the gain boost amplifier is a CMOS  
2 current-input differential amplifier.

1           16.     A differential amplifier circuit comprising:

2                   (a)     first and second supply voltage rails, first and second input terminals, and  
3 an output terminal;

4                   (b)     differentially connected first and second input transistors of a first channel  
5 type;

6                   (c)     a first load transistor of a second channel type coupled between a drain of  
7 the first input transistor and the first supply voltage rail and a second load transistor of the second  
8 channel type coupled between a drain of the second input transistor and the first supply voltage



9 rail; and

10 (d) a gain boost amplifier having a first input coupled to the drain of the first  
11 input transistor, a second input coupled to the drain of the second input transistor, and an output  
12 coupled to gates of the first and second load transistors.

1 17. The differential amplifier circuit of claim 16 including an output stage having an  
2 input coupled to the drain of the first cascode transistor, the output stage including a pull-up  
3 transistor of the second channel type coupled between the second supply voltage rail and the  
4 output terminal, and a second output transistor of the first channel type coupled between the first  
5 supply voltage rail and the output terminal.

1 18. The differential amplifier of claim 17 including a class AB bias circuit coupled  
2 between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

1           19.     The differential amplifier of claim 17 wherein the gain boost amplifier is a CMOS  
2 voltage-input differential amplifier.

1           20.     The differential amplifier of claim 17 wherein the gain boost amplifier is a CMOS  
2 current-input differential amplifier.

1           21.     A method of operating a differential amplifier circuit which includes first and  
2 second supply voltage rails, first and second input terminals, and an output terminal,  
3 differentially connected first and second input transistors of a first channel type, and a folded  
4 cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and  
5 a second cascode transistor both of a second channel type, sources of the first and second cascode  
6 transistors being coupled to drains of the first and second input transistors, respectively, the  
7 sources of the first and second cascode transistors also being coupled to a drain of a first load  
8 transistor and a drain of a second load transistor, respectively, the method comprising:

9           boosting the gain of the differential amplifier circuit without introducing additional  
10 components into a signal path of the differential amplifier circuit by providing local feedback

11 representative of an output voltage of the differential amplifier circuit to gates of the first and  
12 second load transistors by

13 (a) coupling a drain of a third cascode transistor of the second channel type to  
14 a current source circuit and coupling a source of the third cascode transistor to a drain of the  
15 second cascode transistor;

16 (b) coupling a drain of the third cascode transistor to gates of the first and  
17 second load transistors; and

18 (c) driving a gate of the third cascode transistor by means of a gain boost  
19 amplifier having a first input coupled to the drain of the first cascode transistor and a second  
20 input coupled to the drain of the second cascode transistor, to accomplish the function of  
21 increasing the output impedance of the differential amplifier circuit.

1 22. The method of claim 21 wherein step (b) includes driving a gate of the third  
2 cascode transistor by means of a level shift circuit coupled to the drain of the third cascode  
3 transistor.

1           23.     A method of operating a differential amplifier circuit which includes first and  
2 second supply voltage rails, first and second input terminals, and an output terminal,  
3 differentially connected first and second input transistors of a first channel type, and a folded  
4 cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and  
5 a second cascode transistor both of a second channel type, sources of the first and second cascode  
6 transistors being coupled to drains of the first and second input transistors, respectively, the  
7 sources of the first and second cascode transistors also being coupled to a drain of a first load  
8 transistor and a drain of a second load transistor, respectively, the method comprising:

9           boosting the gain of the differential amplifier circuit without introducing additional  
10 components into a signal path of the differential amplifier circuit by providing local feedback  
11 representative of an output voltage of the differential amplifier circuit to gates of the first and  
12 second load transistors by

13           (a)     coupling a first input of a gain boost amplifier to a drain of the first  
14 cascode transistor, and coupling a second input of the gain boost amplifier to a drain of the  
15 second cascode transistor; and

16           (b)     coupling an output of the gain boost amplifier to gates of the first and  
17 second load transistors to drive the first and second load transistors so as to accomplish the  
18 function of increasing the output impedance of the differential amplifier circuit.

1           24.     A method of operating a differential amplifier circuit which includes first and  
2     second supply voltage rails, first and second input terminals, and an output terminal,  
3     differentially connected first and second input transistors of a first channel type, and a folded  
4     cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and  
5     a second cascode transistor both of a second channel type, sources of the first and second cascode  
6     transistors being coupled to drains of the first and second input transistors, respectively, the  
7     sources of the first and second cascode transistors also being coupled to a drain of a first load  
8     transistor and a drain of a second load transistor, respectively, the method comprising:

9           boosting the gain of the differential amplifier circuit without introducing additional  
10    components into a signal path of the differential amplifier circuit by providing local feedback  
11    representative of an output voltage of the differential amplifier circuit to gates of the first and  
12    second load transistors by

13           (a)     coupling a first input of a gain boost amplifier to the source of the first  
14    cascode transistor, and coupling a second input of the gain boost amplifier to the source of the  
15    second cascode transistor;

16           (b)     coupling a drain of the second cascode transistor to gates of the first and  
17    second load transistors; and

18           (c)     coupling an output of the gain boost amplifier to a gate of the second  
19    cascode transistor to cause the drain of the second cascode transistor to drive the gates of the first

20 and second load transistors so as to accomplish the function of increasing the output impedance  
21 of the differential amplifier circuit.

1           25.    A method of operating a differential amplifier circuit which includes first and  
2 second supply voltage rails, first and second input terminals, and an output terminal,  
3 differentially connected first and second input transistors of a first channel type, sources of the  
4 first and second input transistors being coupled to the drain of a first load transistor and a drain of  
5 a second load transistor, respectively, the method comprising:

6           boosting the gain of the differential amplifier circuit by providing local feedback  
7 representative of an output voltage of the differential amplifier circuit to gates of the first and  
8 second load transistors by

9           (a)    coupling a first input of a gain boost amplifier to a drain of the first load  
10 transistor, and coupling a second input of the gain boost amplifier to a drain of the second load  
11 transistor; and

12           (b)    coupling an output of the gain boost amplifier to gates of the first and  
13 second load transistors to drive the first and second load transistors so as to accomplish the  
14 function of increasing the output impedance of the differential amplifier circuit.

1           26.    A current mirror circuit comprising:

2                   (a)    a supply voltage rail, an input terminal, and an output terminal;

3                   (b)    a first transistor and a second transistor;

4                   (c)    a third transistor coupled between a source of the first transistor and the  
5 supply voltage rail and a fourth transistor coupled between a source of the second transistor and  
6 the supply voltage rail;

7                   (d)    a first bias source producing a bias signal on gates of the first and second  
8 transistors, respectively;

9                   (e)    a fifth transistor having a source coupled to a drain of the first transistor  
10 and a drain coupled to the input terminal, a drain of the second transistor being coupled to the  
11 output terminal, and a second bias source coupled to gates of the third and fourth transistors; and

12                   (f)    an amplifier having a first input coupled to the drain of the second  
13 transistor, a second input coupled to the drain of the first transistor, and an output coupled to a  
14 gate of the fifth transistor.